WHAT IS CLAIMED IS:

1. A clock conversion apparatus for converting data synchronized with a first clock into data synchronized with a second clock, said apparatus comprising:

a memory having addresses less than addresses required for storage of data corresponding to a predetermined period, and being able to execute a writing operation and a reading operation independently from each other using a clock for writing and a clock for reading, respectively;

a first counter circuit for counting the first clock, and generating write addresses of the memory so that the data corresponding to the predetermined period can be written into the memory over plural times; and

a second counter circuit for counting the second clock, and generating read addresses of the memory so that the data corresponding to the predetermined period, which have been written in the memory, can be read from the memory over plural times.

2. A clock conversion apparatus for converting data synchronized with a first clock into data synchronized with a second clock, said apparatus comprising:

a memory having addresses less than addresses required for storage of data corresponding to a predetermined period, and being able to execute a writing operation and a reading operation

independently from each other using a clock for writing and a clock for reading, respectively;

a first counter circuit for starting count of the first clock on receipt of a writing start reference signal indicating a reference timing of starting data writing into the memory, and generating write addresses of the memory so that the data corresponding to the predetermined period can be written in the memory over plural times; and

a second counter circuit for starting count of the second clock from a reading start reference signal indicating a reference timing of starting data reading from the memory, and generating read addresses of the memory so that the data corresponding to the predetermined period, which have been written in the memory, can be read over plural times.

3. A clock conversion apparatus for converting data synchronized with a first clock into data synchronized with a second clock, said apparatus comprising:

a memory having addresses less than addresses required for storage of data corresponding to a predetermined period, and being able to execute a writing operation and a reading operation independently from each other using a clock for writing and a clock for reading, respectively;

a first counter circuit for starting count of the first clock on receipt of a writing start reference signal indicating a

reference timing of starting data writing into the memory, and generating write addresses of the memory so that the data corresponding to the predetermined period can be written into the memory over plural times;

a second counter circuit for starting count of the second clock from a reading start reference signal indicating a reference timing of starting data reading from the memory, and generating read addresses of the memory so that the data corresponding to the predetermined period, which have written in the memory, can be read over plural times; and

a delay adjustment circuit capable of adjusting a delay time, which delays the writing start reference signal to generate the reading start reference signal.

4. A clock conversion apparatus for converting data synchronized with a first clock into data synchronized with a second clock, said apparatus comprising:

a memory having addresses less than addresses required for storage of data corresponding to a predetermined period, and being able to execute a writing operation and a reading operation independently from each other using a clock for writing and a clock for reading, respectively;

a first counter circuit for starting count of the first clock on receipt of a writing start reference signal indicating a reference timing of starting data writing into the memory, and

generating write addresses of the memory, which repeat increase or decrease within a predetermined range of addresses of the memory, so that the data corresponding to the predetermined period can be written in the memory over plural times;

a second counter circuit for starting count of the second clock from a reading start reference signal indicating a reference timing of starting data reading from the memory, and generating read addresses of the memory, which repeat increase or decrease within a predetermined range of addresses of the memory, so that the data corresponding to the predetermined period which are written in the memory can be read over plural times; and

a delay adjustment circuit capable of adjusting a delay time, which delays the writing start reference signal to generate the reading start reference signal.

5. A clock conversion apparatus for converting data synchronized with a first clock into data synchronized with a second clock, said apparatus comprising:

a memory having addresses less than addresses required for storage of data corresponding to a predetermined period, and being able to execute a writing operation and a reading operation independently from each other using a clock for writing and a clock for reading, respectively;

a first counter circuit for starting count of the first clock on receipt of a writing start reference signal indicating a

reference timing of starting data writing into the memory, and generating write addresses of the memory so that the write addresses repeat increase or decrease within a predetermined range of addresses of the memory, and the last increase or decrease for every predetermined period is carried out within a range of addresses narrower than the predetermined range of addresses, thereby enabling writing of the data corresponding to the predetermined period into the memory over plural times;

a second counter circuit for starting count of the second clock from a reading start reference signal indicating a reference timing of starting data reading from the memory, and generating read addresses of the memory so that the read addresses repeat increase or decrease within a predetermined range of addresses of the memory, and the last increase or decrease for every predetermined period is carried out within a range of addresses narrower than the predetermined range of addresses, thereby enabling reading of the data corresponding to the predetermined period, which have been written in the memory, over plural times; and

a delay adjustment circuit capable of adjusting a delay time, which delays the writing start reference signal to generate the reading start reference signal.

6. A clock conversion apparatus as defined in any of Claims 1 to 5 wherein

the data corresponding to the predetermined period are written in the memory using such write addresses that a multiple of a maximum write address value becomes close to the number of samples of data that are sampled at the first clock within the predetermined period; and

the data are read from the memory using such read addresses that a multiple of a maximum read address value becomes close to the number of samples of data that are sampled at the second clock.

7. A clock conversion apparatus as defined in any of Claims 1 to 5 wherein

the data corresponding to the predetermined period are written in the memory using such write addresses that a multiple of a maximum write address value becomes close to the number of samples of data that are sampled at the first clock within the predetermined period; and

the data are read from the memory using read addresses having a maximum value equal to the maximum value of the write addresses.

8. A clock conversion apparatus as defined in any of Claims 1 to 5 wherein

the predetermined period is one horizontal sync period.

9. A clock conversion apparatus as defined in any of Claims 1 to

5 wherein

the first counter circuit comprises:

a write address counter for counting the first clock to create the write addresses; and

a write maximum value limiter for comparing the write address outputted from the write address counter with a settable write maximum value, and resetting the write address counter when the write address becomes equal to the write maximum value.

10. A clock conversion apparatus as defined in any of Claims 1 to 5 wherein

the second counter circuit comprises:

a read address counter for counting the second clock to create the read addresses; and

a read maximum value limiter for comparing the read address outputted from the read address counter with a settable read maximum value, and resetting the read address counter when the read address becomes equal to the read maximum value.

11. A clock conversion method for converting data synchronized with a first clock into data synchronized with a second clock, said method comprising:

generating write addresses on the basis of the first clock so that data corresponding to a predetermined period are written over plural times into a memory which has addresses less than

addresses required for storage of the data corresponding to the predetermined period, and is able to execute a writing operation and a reading operation independently from each other using a clock for writing and a clock for reading, respectively; and

generating read addresses on the basis of the second clock so that the data corresponding to the predetermined period are read from the memory over plural times.

12. A video display apparatus comprising:

a first video processing unit for subjecting a digital video signal to first video processing on the basis of a first clock;

a clock conversion unit for converting the digital video signal which is outputted from the first video processing unit and synchronized with the first clock into a digital video signal synchronized with a second clock;

a second video processing unit for subjecting the digital video signal outputted from the clock conversion unit to second video processing on the basis of the second clock;

a display device for displaying the digital video signal outputted from the second video processing unit; and

said clock conversion unit comprising:

a memory having a capacity less than one horizontal line of the digital video signal outputted from the first video processing unit, and being able to execute a writing operation and a reading operation independently from each other using a

clock for writing and a clock for reading, respectively; and

a memory controller for controlling the memory so that the digital video signal outputted from the first video processing unit are written into the memory over plural times for every horizontal line, and the data corresponding to each horizontal line, which are written in the memory, can be read over plural times.

13. A video display apparatus as defined in Claim 12, wherein said memory controller comprises:

a first counter circuit for starting count of the first clock on receipt of a writing start reference signal indicating a reference timing of starting data writing into the memory, and generating write addresses of the memory so that the one horizontal line of data can be written into the memory over plural times; and

a second counter circuit for starting count of the second clock from a reading start reference signal indicating a reference timing of starting data reading from the memory, and generating read addresses of the memory so that the one horizontal line of data which are written in the memory can be read over plural times.

14. A memory address setting method for a video display apparatus comprising:

a first video processing unit for subjecting a digital video signal to first video processing on the basis of a first clock;

a clock conversion unit for converting the digital video signal which is outputted from the first video processing unit and synchronized with the first clock into a digital video signal synchronized with a second clock;

a second video processing unit for subjecting the digital video signal outputted from the clock conversion unit to second video processing on the basis of the second clock;

a display device for displaying the digital video signal outputted from the second video processing unit; and

said clock conversion unit comprising:

a memory having addresses less than addresses required for storage of data corresponding to a predetermined period, and being able to execute a writing operation and a reading operation independently from each other using a clock for writing and a clock for reading, respectively;

a first counter circuit for generating write addresses of the memory on the basis of the first clock so that the data corresponding to the predetermined period are written over plural times; and

a second counter circuit for generating read addresses of the memory on the basis of the second clock so that the data corresponding to the predetermined period are from the memory over plural times; and

said memory address setting method comprising:

a step of determining a broadcasting system of the digital video signal inputted to the first video processing unit;

a step of detecting upper limits or lower limits of count values of the first and second counter circuits corresponding to the determined broadcasting system, according to the broadcasting system; and

a step of setting the detected upper limits or lower limits of the count values on the first and second counter circuits.